EAST SEARCH

1/25/2007

L#	Hits	Search String	Databases
S2	3425	S1 and ("computer aided design" or CAD)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S3	236	S2 and (data near2 (model or version))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S1	28150	(integrated near2 circuit) with design	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S4	36	S2 and ((data near2 (model or version)) with (consisten$2 or compatibility or compatible or cc	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S27	383	S4 or S6 or S8 or S9 or S10 or S11 or S12 or S14 or S17 or S18 or S19 or S21 or S24 or S2!	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S6	73	S2 and ((data with (model or version)) with (consisten$2 or compatibility or compatible or corr	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S9	5	S2 and ((data with (model or version)) with ((current or previous) near2 version))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S7	414	S2 and ((consisten$2 or compatibility or compatible or correct$4 or valid$3) with (indicator or information or database))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S8	139	S2 and ((consisten$2 or compatibility or compatible or correct$4 or valid$3) with (indicator or database))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S10	69	S2 and (data with version)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S11	5	S2 and ((data with (model or version)) with block with (consisten$2 or compatibility or compat	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S13	0	S2 and ((consisten$2 or compatibility or compatible or correct$4 or valid$3) with (timestamp c	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S12	58	S2 and (compar$4 with (data with (field or value)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S19	27	S2 and (difference with (data with (field or value)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S26	2	S2 and ((file near2 size) with (verif$4 or validat$3 or check$3 or compar$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S14	23	S2 and (timestamp or (time near2 (creation or modification)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S5	557	S2 and (data with (model or version))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S17	1	S2 and ((inconsisten$2 or incompatibility or incompatible or incorrect$4 or invalid$3) with war	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S16	0	S2 and (data with discrepancy)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S15	0	S2 and (discrepancy with warning)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S18	10	S2 and (data with warning)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S20	0	S2 and ((consisten$2 or compatibility or compatible or correct$4 or valid$3) with (file near2 si	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S21	13	S2 and (data with (file near2 size))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S24	67	S2 and ((data with (model or version)) with (verif$4 or validat$3 or check$3 or compar$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S25	3	S2 and ((timestamp or (time near2 (creation or modification))) with (verif$4 or validat$3 or che	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S23	0	S2 and (source with (file near2 size))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S22	0	S2 and ((source near2 file) with (file near2 size))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S30	264	S28 or S29	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S29	20	S8 and S28	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S28	264	S4 or S6 or S9 or S10 or S11 or S12 or S14 or S17 or S18 or S19 or S21 or S24 or S25 or S2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S33	17	S31 and (compar$4 near2 ((data or file) near2 (timestamp or (creation near2 time) or (modific	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S34	1089	S32 or S33	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S32	1072	S31 and (compar$4 near2 ((data near2 time) or (data near2 timing) or (data near2 version) o	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S31	907174	("integrated circuit" or simulat$3 or "computer aided design")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S35	60	S34 and ((discrepancy or differen$2) with (message or warning))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S46	10	S37 and (data with warning)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S47	27	S37 and (difference with (data with (field or value)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S48	13	S37 and (data with (file near2 size))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S49	67	S37 and ((data with (model or version)) with (verif$4 or validat$3 or check$3 or compar$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB

S39	73	S37 and ((data with (model or version)) with (consisten$2 or compatibility or compatible or co	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S43	58	S37 and (compar$4 with (data with (field or value)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S50	3	S37 and ((timestamp or (time near2 (creation or modification))) with (verif$4 or validat$3 or cl	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S45	1	S37 and ((inconsisten$2 or incompatibility or incompatible or incorrect$4 or invalid$3) with wa	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S38	36	S37 and ((data near2 (model or version)) with (consisten$2 or compatibility or compatible or c	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S51	2	S37 and ((file near2 size) with (verif$4 or validat$3 or check$3 or compar$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S37	3425	S36 and ("computer aided design" or CAD)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S53	907174	("integrated circuit" or simulat$3 or "computer aided design")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S44	23	S37 and (timestamp or (time near2 (creation or modification)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S54	1072	S53 and (compar$4 near2 ((data near2 time) or (data near2 timing) or (data near2 version) o	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S55	17	S53 and (compar$4 near2 ((data or file) near2 (timestamp or (creation near2 time) or (modific	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S40	5	S37 and ((data with (model or version)) with ((current or previous) near2 version))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S41	69	S37 and (data with version)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S42	5	S37 and ((data with (model or version)) with block with (consisten$2 or compatibility or compa	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S56	1089	S54 or S55	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S36	28150	(integrated near2 circuit) with design	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S52	264	S38 or S39 or S40 or S41 or S42 or S43 or S44 or S45 or S46 or S47 or S48 or S49 or S50 c	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S57	60	S56 and ((discrepancy or differen$2) with (message or warning))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S58	13	S52 and S48	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S59	2	S37 and (compar$4 with (file near2 size))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB

10647769 **Brandon Keller et al.**

EAST SEARCH

1/25/2007

Results of search set S91:

Document Kind Codes	Title	Issue Date	Current OR	Abstract
US 20060195311 A1	Synchronizing On-Chip Data Processor Trace and Timing Information for Export	20060831	703/26	
US 20060193508 A1	Pattern measuring method and pattern measuring device	20060831	382/145	
US 20060190921 A1	Manufacturing Method of Semiconductor Device	20060824	716/21	
US 20060161874 A1	Printed circuit wiring board designing support device, printed circuit board designing method,	20060720	716/8	
US 20060122818 A1	Method, system and program product for defining and recording threshold-qualified count eve	20060608	703/17	
US 20060112376 A1	Virtual data representation through selective bidirectional translation	20060525	717/136	
US 20060109032 A1	Method and apparatus for verifying semiconductor integrated circuits	20060525	327/41	
US 20060089827 A1	Method, system and program product for defining and recording minium and maximum event	20060427	703/17	
US 20060089826 A1	Method, system and program product for defining and recording minimum and maximum cou	20060427	703/17	
US 20060069958 A1	Defect location identification for microdevice manufacturing and test	20060330	714/33	
US 20060066339 A1	Determining and analyzing integrated circuit yield and quality	20060330	324/765	
US 20060066338 A1	Fault dictionaries for integrated circuit yield and quality analysis methods and systems	20060330	324/765	
US 20060062445 A1	Methods, systems, and carrier media for evaluating reticle layout data	20060323	382/144	
US 20060059447 A1	Integrated circuit design support apparatus, integrated circuit design support method, and inte	20060316	716/10	
US 20060059387 A1	Processor condition sensing circuits, systems and methods	20060316	714/30	
US 20060053357 A1	Integrated circuit yield and quality analysis methods and systems	20060309	714/742	
US 20060036977 A1	Physical design system and method	20060216	716/4	
US 20060026017 A1	National / international management and security system for responsible global resourcing thi	20060202	705/1	

US 20060015829 A1	Method and apparatus for designing electronic circuits using optimization	20060119	716/2
US 20060005154 A1	Integrated OPC verification tool	20060105	716/5
US 20050229124 A1	Distributed BDD reordering	20051013	716/5
US 20050210437 A1	Method of manufacturing reliability checking and verification for lithography process using a c	20050922	716/19
US 20050179886 A1	Method of predicting and minimizing model OPC deviation due to mix/match of exposure tool	20050818	355/77
US 20050165995 A1	System of distributed microprocessor interfaces toward macro-cell based designs implemente	20050728	710/305
US 20050160388 A1	Streamlined IC mask layout optical and process correction through correction reuse	20050721	716/5
US 20050149313 A1	Method and system for selective compilation of instrumentation entities into a simulation mod	20050707	703/22
US 20050149309 A1	Method, system and program product supporting user tracing in a simulator	20050707	703/14
US 20050148115 A1	Programmed material consolidation methods for fabricating heat sinks	20050707	438/122
US 20050146714 A1	Pattern inspection apparatus and method	20050707	356/237.2
US 20050132316 A1	Retiming circuits using a cut-based approach	20050616	716/11
US 20050120316 A1	Mutual inductance extraction using dipole approximations	20050602	716/4
US 20050086566 A1	System and method for building a test case including a summary of instructions	20050421	714/741
US 20050076316 A1	Design-manufacturing interface via a unified model	20050407	716/4
US 20050065903 A1	Methods and apparatus for information hyperchain management for on-demand business col	20050324	707/1
US 20050050481 A1	Systems and methods for determining activity factors of a circuit design	20050303	716/4
US 20050004774 A1	Methods and systems for inspection of wafers and reticles using designer intent data	20050106	702/108
US 20040236547 A1	System and method for automated placement or configuration of equipment for obtaining des	20041125	703/2
US 20040143428 A1	System and method for automated placement or configuration of equipment for obtaining des	20040722	703/22
US 20040139419 A1	Minimization of microelectronic interconnect thickness variations	20040715	716/20
US 20040109059 A1	Hybrid joint photographer's experts group (JPEG) /moving picture experts group (MPEG) spe	20040610	348/143
US 20040093397 A1	Isolated working chamber associated with a secure inter-company collaboration environment	20040513	709/219
US 20040086791 A1	Photomask defect testing method, photomask manufacturing method and semiconductor inte	20040506	430/5
US 20040078767 A1	Representing the design of a sub-module in a hierarchical integrated circuit design and analy	20040422	716/8
US 20040064797 A1	Pure fill via area extraction in a multi-wide object class design layout	20040401	716/5
US 20040064796 A1	Correction of spacing violations between pure fill via areas in a multi-wide object class design	20040401	716/5
US 20040064795 A1	Via enclosure rule check in a multi-wide object class design layout	20040401	716/5
US 20040040004 A1	Cell library database and timing verification and withstand voltage verification systems for inte	20040226	716/4
US 20040036161 A1	Heat sinks including nonlinear passageways	20040226	257/706
US 20040031005 A1	Electronic cad system and layout data producing method therefor	20040212	716/8
US 20040019862 A1	Structure and method for separating geometries in a design layout into multi-wide object clas	20040129	716/5
US 20040015808 A1	System and method for providing defect printability analysis of photolithographic masks with j	20040122	716/19
US 20040015790 A1	Method of designing and making an integrated circuit	20040122	716/3
US 20030237067 A1	System and method for applying timing models in a static-timing analysis of a hierarchical inte	20031225	716/6
US 20030229860 A1	Method, system and computer product to produce a computer-generated integrated circuit de	20031211	716/1
US 20030229482 A1	Apparatus and method for managing integrated circuit designs	20031211	703/14
US 20030223630 A1	Overlay metrology and control method	20031204	382/145
US 20030211657 A1	Stereolithographic method for fabricating heat sinks, stereolithographically fabricated heat sin	20031113	438/122
US 20030208730 A1	Method for verifying properties of a circuit model	20031106	716/4
US 20030200071 A1	Simulation method	20031023	703/15
US 20030196144 A1	Processor condition sensing circuits, systems and methods	20031016	714/34
US 20030192025 A1	Automated flow in PSM phase assignment	20031009	716/19
US 20030191869 A1	C-API instrumentation for HDL models	20031009	719/328
US 20030191621 A1	Method and system for reducing storage and transmission requirements for simulation results	20031009	703/17
US 20030191620 A1	Dynamic loading of C-API HDL model instrumentation	20031009	703/17
US 20030191618 A1	Method and system for reducing storage requirements of simulation data via keyword restricti	20031009	703/13
US 20030191617 A1	Method and system for selectively storing and retrieving simulation data utilizing keywords	20031009	703/13

US 20030188277 A1	Method of evaluating semiconductor integrated circuit to be designed in consideration of stan	20031002	716/4
US 20030179625 A1	Clock phase adjustment method, integrated circuit, and method for designing the integrated c	20030925	365/200
US 20030138706 A1	Binary half tone photomasks and microscopic three-dimensional devices and method of fabri	20030724	430/5
US 20030135354 A1	Tracking converage results in a batch simulation farm network	20030717	703/13
US 20030126582 A1	Pattern correction method and manufacturing method of semiconductor device	20030703	716/21
US 20030125915 A1	Count data access in a distributed simulation environment	20030703	703/13
US 20030101382 A1	Fail thresholding in a batch simulation farm network	20030529	714/39
US 20030101307 A1	System of distributed microprocessor interfaces toward macro-cell based designs implemente	20030529	710/305
US 20030101041 A1	Annealing harvest event testcase collection within a batch simulation farm	20030529	703/22
US 20030101039 A1	Maintaining data integrity within a distributed simulation environment	20030529	703/16
US 20030101038 A1	Centralized disablement of instrumentation events within a batch simulation farm network	20030529	703/16
US 20030101035 A1	Non-redundant collection of harvest events within a batch simulation farm network	20030529	703/13
US 20030088839 A1	Method of designing integrated circuit and apparatus for designing integrated circuit	20030508	716/7
US 20030082463 A1	Method of two dimensional feature model calibration and optimization	20030501	430/5
US 20030074153 A1	Application specific event based semiconductor memory test system	20030417	702/122
US 20030056163 A1	Method of evaluating core based system-on-a-chip	20030320	714/724
US 20030051222 A1	Integrated circuit chip design	20030313	716/12
US 20030018949 A1	Method and apparatus for laying out wires on a semiconductor integrated circuit	20030123	716/14
US 20030018948 A1	Method and apparatus for data hierarchy maintenance in a system for mask description	20030123	716/8
US 20030001171 A1	Semiconductor integrated circuit having macro cells and designing method of the same	20030102	257/207
US 20020194558 A1	Method and system to optimize test cost and disable defects for scan and BIST memories	20021219	714/718
US 20020166107 A1	Method and apparatus for generating masks utilized in conjunction with dipole illumination tec	20021107	716/19
US 20020161947 A1	Route searching method, timing analyzing method, waveform analyzing method, electronic ci	20021031	710/38
US 20020143510 A1	Integrated circuit I/O pad cell modeling	20021003	703/14
US 20020105049 A1	Integrated circuit having tap cells and a method for positioning tap cells in an integrated circui	20020808	257/511
US 20020093356 A1	Intelligent test vector formatting to reduce test vector size and allow encryption thereof for inte	20020718	324/765
US 20020026627 A1	Streamlined IC mask layout optical and process correction through correction reuse	20020228	716/19
US 20010053964 A1	METHOD OF FORMING A PATTERN USING PROXIMITY-EFFECT-CORRECTION	20011220	703/2
US 20010044667 A1	System of manufacturing semiconductor intergrated circuit	20011122	700/100
US 20010007972 A1	Method and apparatus for verifying adequacy of test patterns	20010712	703/16
US 7093229 B2	System and method for providing defect printability analysis of photolithographic masks with j	20060815	716/21
US 7092868 B2	Annealing harvest event testcase collection within a batch simulation farm	20060815	703/22
US 7086019 B2	Systems and methods for determining activity factors of a circuit design	20060801	716/4
US 7085703 B2	Count data access in a distributed simulation environment	20060801	703/17
US 7076752 B2	System and method for determining unmatched design elements in a computer-automated de	20060711	716/5
US 7073153 B2	Route searching method and storage medium thereof	20060704	716/13
US 7073152 B2	System and method for determining a highest level signal name in a hierarchical VLSI design	20060704	716/12
US 7072818 B1	Method and system for debugging an electronic system	20060704	703/14
US 7069526 B2	Hardware debugging in a hardware description language	20060627	716/4
US 7065739 B2	Pattern correction method of semiconductor device	20060620	716/21
US 7065481 B2	Method and system for debugging an electronic system using instrumentation circuitry and a l	20060620	703/14
US 7062727 B2	Computer aided design systems and methods with reduced memory utilization	20060613	716/1
US 7058908 B2	Systems and methods utilizing fast analysis information during detailed analysis of a circuit de	20060606	716/4
US 7055135 B2	Method for debugging an integrated circuit	20060530	717/124
US 7051301 B2	System and method for building a test case including a summary of instructions	20060523	716/4
US 7047507 B2	System and method for determining wire capacitance for a VLSI circuit	20060516	716/5
US 7039566 B2	Method of estimating a lifetime of hot carrier of MOS transistor, and simulation of hot carrier d	20060502	703/2
US 7037627 B2	Photomask defect testing method, photomask manufacturing method and semiconductor inte	20060502	430/5

US 7032206 B2	System and method for iteratively traversing a hierarchical circuit design	20060418	716/12
US 7028284 B2	Convergence technique for model-based optical and process correction	20060411	716/21
US 7027971 B2	Centralized disablement of instrumentation events within a batch simulation farm network	20060411	703/14
US 7026191 B2	Stereolithographic method for fabricating heat sinks, stereolithographically fabricated heat sin	20060411	438/122
US 7024655 B2	Mixed-mode optical proximity correction	20060404	716/19
US 7020856 B2	Method for verifying properties of a circuit model	20060328	716/4
US 7007249 B2	Method for automatically generating checkers for finding functional defects in a description of	20060228	716/4
US 6996515 B1	Enabling verification of a minimal level sensitive timing abstraction model	20060207	703/19
US 6993728 B2	Method of designing integrated circuit and apparatus for designing integrated circuit	20060131	716/1
US 6983440 B1	Shape abstraction mechanism	20060103	716/11
US 6978012 B2	Echo cancellation using a variable offset comparator	20051220	379/406.01
US 6976232 B2	Method of designing and making an integrated circuit	20051213	716/3
US 6970966 B2	System of distributed microprocessor interfaces toward macro-cell based designs implemente	20051129	710/305
US 6954907 B2	System of manufacturing semiconductor integrated circuit by having a client connected to a m	20051011	716/1
US 6947883 B1	Method for designing mixed signal integrated circuits and configurable synchronous digital nc	20050920	703/23
US 6944808 B2	Method of evaluating core based system-on-a-chip	20050913	714/724
US 6934900 B1	Test pattern generator for SRAM and DRAM	20050823	714/738
US 6934885 B2	Fail thresholding in a batch simulation farm network	20050823	714/33
US 6934671 B2	Method and system for including parametric in-line test data in simulations for improved mode	20050823	703/14
US 6931572 B1	Design instrumentation circuitry	20050816	714/34
US 6925621 B2	System and method for applying timing models in a static-timing analysis of a hierarchical inte	20050802	716/6
US 6920620 B2	Method and system for creating test component layouts	20050719	716/4
US 6918100 B2	Hierarchical evaluation of cells	20050712	716/4
US 6907596 B2	Mask data generating apparatus, a computer implemented method for generating mask data	20050614	716/19
US 6904578 B2	System and method for verifying a plurality of states associated with a target circuit	20050607	716/5
US 6904577 B2	Hardware debugging in a hardware description language	20050607	716/4
US 6895568 B2	Correction of spacing violations between pure fill via areas in a multi-wide object class design	20050517	716/10
US 6883153 B2	Minimization of microelectronic interconnect thickness variations	20050419	716/6
US 6883149 B2	Via enclosure rule check in a multi-wide object class design layout	20050419	716/4
US 6873720 B2	System and method of providing mask defect printability analysis	20050329	382/149
US 6871332 B2	Structure and method for separating geometries in a design layout into multi-wide object class	20050322	716/5
US 6868374 B1	Method of power distribution analysis for I/O circuits in ASIC designs	20050315	703/18
US 6853589 B2	Clock phase adjustment method, integrated circuit, and method for designing the integrated c	20050208	365/189.05
US 6832360 B2	Pure fill via area extraction in a multi-wide object class design layout	20041214	716/5
US 6828068 B2	Binary half tone photomasks and microscopic three-dimensional devices and method of fabri	20041207	430/5
US 6823497 B2	Method and user interface for debugging an electronic system	20041123	716/4
US 6810509 B2	Method of evaluating semiconductor integrated circuit to be designed in consideration of stan	20041026	716/4
US 6785873 B1	Emulation system with multiple asynchronous clocks	20040831	716/4
US 6775806 B2	Method, system and computer product to produce a computer-generated integrated circuit de	20040810	716/1
US 6766506 B1	Interconnect model compiler	20040720	716/18
US 6766504 B1	Interconnect routing using logic levels	20040720	716/13
US 6763511 B2	Semiconductor integrated circuit having macro cells and designing method of the same	20040713	716/12
US 6748578 B2	Streamlined IC mask layout optical and process correction through correction reuse	20040608	716/19
US 6732340 B1	Method for designing a semiconductor integrated circuit which includes consideration of para	20040504	716/5
US 6730998 B1	Stereolithographic method for fabricating heat sinks, stereolithographically fabricated heat sin	20040504	257/712
US 6728946 B1	Method and apparatus for creating photolithographic masks	20040427	716/19
US 6704921 B2	Automated flow in PSM phase assignment	20040309	716/19
US 6704695 B1	Interactive optical proximity correction design method	20040309	703/6

US 6687710 B1	Intellectual property library management system	20040203	705/36R
US 6631340 B2	Application specific event based semiconductor memory test system	20031007	702/122
US 6629282 B1	Module based flexible semiconductor test system	20030930	714/734
US 6606735 B1	Method and system for using error and filter layers in each DRC rule	20030812	716/5
US 6584455 B1	System and method for predicting design errors in integrated circuits	20030624	706/45
US 6581191 B1	Hardware debugging in a hardware description language	20030617	716/4
US 6563114 B1	Substrate inspecting system using electron beam and substrate inspecting method using elec	20030513	250/310
US 6560755 B1	Apparatus and methods for modeling and simulating the effect of mismatch in design flows of	20030506	716/4
US 6560753 B2	Integrated circuit having tap cells and a method for positioning tap cells in an integrated circui	20030506	716/2
US 6560568 B1	Deriving statistical device models from electrical test data	20030506	703/2
US 6556505 B1	Clock phase adjustment method, and integrated circuit and design method therefor	20030429	365/233
US 6553562 B2	Method and apparatus for generating masks utilized in conjunction with dipole illumination tec	20030422	716/19
US 6553548 B1	System and method for recovering from design errors in integrated circuits	20030422	716/5
US 6543039 B1	Method of designing integrated circuit and apparatus for designing integrated circuit	20030401	716/7
US 6541285 B2	Method of estimating lifetime of semiconductor device, and method of reliability simulation	20030401	438/14
US 6536006 B1	Event tester architecture for mixed signal testing	20030318	714/724
US 6532561 B1	Event based semiconductor test system	20030311	714/738
US 6480817 B1	Integrated circuit I/O pad cell modeling	20021112	703/15
US 6470489 B1	Design rule checking system and method	20021022	716/21
US 6453452 B1	Method and apparatus for data hierarchy maintenance in a system for mask description	20020917	716/8
US 6453274 B2	Method of forming a pattern using proximity-effect-correction	20020917	703/2
US 6421823 B1	Bidirectional socket stimulus interface for a logic simulator	20020716	717/135
US 6377912 B1	Emulation system with time-multiplexed interconnect	20020423	703/28
US 6370679 B1	Data hierarchy layout correction and verification method and apparatus	20020409	716/19
US 6370675 B1	Semiconductor integrated circuit design and evaluation system using cycle base timing	20020409	716/6
US 6363509 B1	Method and apparatus for transforming system simulation tests to test patterns for IC testers	20020326	714/738
US 6360353 B1	Automated alternating current characterization testing	20020319	716/4
US 6342794 B1	Interface for low-voltage semiconductor devices	20020129	326/68
US 6341366 B1	Rule-driven method and system for editing physical integrated circuit layouts	20020122	716/11
US 6331770 B1	Application specific event based semiconductor test system	20011218	324/158.1
US 6327556 B1	AT-speed computer model testing methods	20011204	703/13
US 6314034 B1	Application specific event based semiconductor memory test system	20011106	365/201
US 6304837 B1	Automated test vector generation and verification	20011016	703/14
US 6301697 B1	Streamlined IC mask layout optical and process correction through correction reuse	20011009	716/19
US 6282694 B1	IC design floorplan generation using ceiling and floor contours on an O-tree structure	20010828	716/10
US 6275604 B1	Method and apparatus for generating semiconductor exposure data	20010814	382/146
US 6249891 B1	High speed test pattern evaluation apparatus	20010619	714/738
US 6247165 B1	System and process of extracting gate-level descriptions from simulation tables for formal ver	20010612	716/5
US 6223142 B1	Method and system for incrementally compiling instrumentation into a simulation model	20010424	703/15
US 6219630 B1	Apparatus and method for extracting circuit, system and method for generating information fo	20010417	703/14
US 6212493 B1	Profile directed simulation used to target time-critical crossproducts during random vector tes	20010403	703/22
US 6152612 A	System and method for system level and circuit level modeling and design simulation using C	20001128	703/23
US 6117182 A	Optimum buffer placement for noise avoidance	20000912	716/8
US 6115034 A	Step managing apparatus and method	20000905	715/700
US 6099578 A	Method of estimating wire length including correction and summation of estimated wire length	20000808	716/4
US 6093212 A	Method for selecting operation cycles of a semiconductor IC for performing an IDDQ test by u	20000725	703/14
US 6080204 A	Method and apparatus for contemporaneously compiling an electronic circuit design by conte	20000627	716/7
US 6061283 A	Semiconductor integrated circuit evaluation system	20000509	365/201

US 6058492 A	Method and apparatus for design verification using emulation and simulation	20000502	714/33
US 6044211 A	Method for graphically representing a digital device as a behavioral description with data and	20000328	716/18
US 6026220 A	Method and apparatus for incremntally optimizing a circuit design	20000215	703/23
US 6009251 A	Method and system for layout verification of an integrated circuit design with reusable subdes	19991228	716/5
US 5960191 A	Emulation system with time-multiplexed interconnect	19990928	703/28
US 5956257 A	Automated optimization of hierarchical netlists	19990921	716/3
US 5936868 A	Method for converting an integrated circuit design for an upgraded process	19990810	716/4
US 5903312 A	Micro-architecture of video core for MPEG-2 decoder	19990511	375/240.03
US 5867399 A	System and method for creating and validating structural description of electronic system fron	19990202	716/18
US 5841967 A	Method and apparatus for design verification using emulation and simulation	19981124	714/33
US 5838583 A	Optimized placement and routing of datapaths	19981117	716/9
US 5828581 A	Automatic layout system	19981027	716/12
US 5822511 A	Smart compare tool and method	19981013	714/8
US 5818532 A	Micro architecture of video core for MPEG-2 decoder	19981006	375/240.03
US 5815685 A	Apparatus and method for correcting light proximity effects by predicting mask performance	19980929	716/21
US 5801958 A	Method and system for creating and validating low level description of electronic design from	19980901	716/18
US 5761664 A	Hierarchical data model for design automation	19980602	707/100
US 5754454 A	Method for determining functional equivalence between design models	19980519	702/123
US 5689432 A	Integrated circuit design and manufacturing method and an apparatus for designing an integr	19971118	716/18
US 5677916 A	Semiconductor integrated circuit and its application device	19971014	714/733
US 5675728 A	Apparatus and method identifying false timing paths in digital circuits	19971007	714/28
US 5646422 A	Semiconductor integrated circuit device	19970708	257/48
US 5623418 A	System and method for creating and validating structural description of electronic system	19970422	716/1
US 5621653 A	Method of and an apparatus for converting layout data in conductive portions	19970415	716/3
US 5559997 A	System and method for designing a printed-circuit board	19960924	716/1
US 5555201 A	Method and system for creating and validating low level description of electronic design from	19960910	716/1
US 5539652 A	Method for manufacturing test simulation in electronic circuit design	19960723	703/14
US 5513119 A	Hierarchical floorplanner for gate array design layout	19960430	716/8
US 5490083 A	Method and apparatus for classifying and evaluating logic circuit	19960206	716/4
US 5416722 A	System and method for compacting integrated circuit layouts	19950516	716/2
US 5416719 A	Computerized generation of truth tables for sequential and combinatorial cells	19950516	716/2
US 5392220 A	Method and system for organizing data	19950221	716/2
US 5390189 A	Semiconductor integrated circuit	19950214	714/728
US 5359535 A	Method for optimization of digital circuit delays	19941025	716/6
US 5331275 A	Probing device and system for testing an integrated circuit	19940719	324/757
US 5315534 A	Computer process for interconnecting logic circuits utilizing softwire statements	19940524	716/12
US 5278770 A	Method for generating input data for an electronic circuit simulator	19940111	703/14
US 5247455 A	Method of verifying wiring layout	19930921	716/15
US 5224055 A	Machine for circuit design	19930629	716/11
US 5214753 A	Video system with parallel attribute interpolations	19930525	345/610
US 5151867 A	Method of minimizing sum-of-product cases in a heterogeneous data base environment for ci	19920929	716/18
US 5150308 A	Parameter and rule creation and modification mechanism for use by a procedure for synthesi	19920922	716/18
US 5128878 A	Remote plotting of integrated circuit layout in a network computer-aided design system	19920707	345/502
US 5084824 A	Simulation model generation from a physical data base of a combinatorial circuit	19920128	716/11
US 5051938 A	Simulation of selected logic circuit designs	19910924	703/15
US 4974175 A	Drawing information processing method and apparatus	19901127	345/619
US 4817012 A	Method for identification of parasitic transistor devices in an integrated structure	19890328	716/5
US 4754432 A	Nonvolatile multiconfigurable circuit	19880628	365/185.08

US 4649474 A	Chip topography for a MOS disk memory controller circuit	19870310	710/5
US 4527249 A	Simulator system for logic design validation	19850702	703/15
JP 2005050066 A	Computer aided design data conversion method for electronic circuit board manufacture, invc	20050224	
JP 2005050065 A	Computer aided design data conversion method for electronic circuit board manufacture, invc	20050224	
JP 2005050071 A	Computer aided design data conversion method for electronic circuit board manufacture, invc	20050224	
EP 856804 A	Step managing appts for designing complex object of design e.g. integrated circuit in CAD sy:	19980805	